512K x 32 SRAM MODULE

PUMA 68S16000X - 12/15/20/25

Issue 1.3 : December 1998

Description

The PUMA68S16000X is a 16Mbit CMOS High Speed Static RAM organised as 512K x 32 in a JEDEC 68 pin surface mount J-leaded PLCC, available with access times of 12, 15, 20 and 25ns. The output width is user configurable as 8, 16 or 32 bits using four Chip Selects ($\overline{CS1}$~4).

The device features multiple ground pins for maximum noise immunity and TTL compatible inputs and outputs. The PUMA 68S16000X is a direct upgrade path from the PUMA 68S4000X and offers a dramatic space saving advantage over four standard 512Kx8 devices.
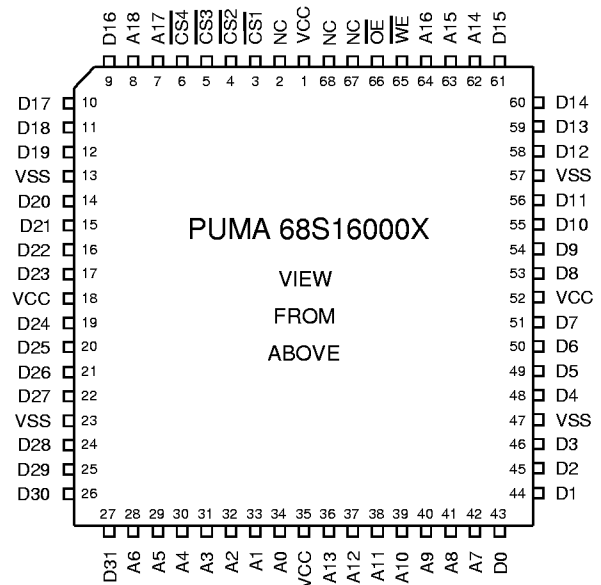
Features

- Very fast access times of 12/15/20/25 ns.

- JEDEC 68 'J' leaded plastic Surface Mount Package.

- User Configurable as 8 / 16 / 32 bit wide output.

- Operating Power   (32-BIT)   4.18 W (max)
  Low Power Standby   (TTL)   1.10 W (max)
                                     (CMOS)   220 mW (max)

- Fully Static operation.

- Multiple ground pins for maximum noise immunity.

- Single 5V±10% Power supply.

Block Diagram
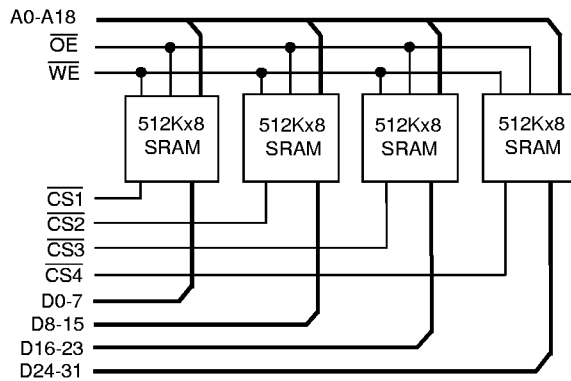
Pin Functions

Address Inputs	A0 - A18
Data Input/Output	D0 - D31
Chip Select	$\overline{CS1}$~4
Write Enable	$\overline{WE}$
Output Enable	$\overline{OE}$
No Connect	NC
Power (+5V)	V$_{cc}$
Ground	GND

Pin Definition

Package Details

Plastic 68 J-Leaded JEDEC PLCC

DC OPERATING CONDITIONS

Absolute Maximum Ratings [1]

Voltage on any pin relative to GND	V_T	-0.3 to +7.0	V
Power Dissipation	P_T	4.0	W
Storage Temperature	T_{STG}	-55 to +125	°C

Notes (1) Stresses above those listed may cause permanent damage. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Units	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5	V	
Input Low Voltage	V_{IL} [1]	-0.3	-	0.8	V	
Operating Temperature	T_A	0	-	70	°C	
	T_{AI}	-40	-	85	°C	(Suffix I)

Notes: (1) Pulse width: -2.0V for less than 10ns.

DC Electrical Characteristics (V_{CC}=5V±10%, T_A=-40°C to +85°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI1}	V_{IN}=0V to V_{CC}	-8	-	8	µA
Output Leakage Current	I_{LO}	$V_{I/O}$=0V to V_{CC}	-8	-	8	µA
Average Supply Current[2] 32 bit	I_{CC32}	$\overline{CS}$[1]=V_{IL}, $I_{I/O}$=0mA, f=f_{max}	-	-	760	mA
16 bit	I_{CC16}	As above.	-	-	480	mA
8 bit	I_{CC8}	As above.	-	-	340	mA
Standby Supply Current (TTL)	I_{SB}	$\overline{CS}$[1]=V_{IH}, Min. cycle	-	-	200	mA
(CMOS)	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, 0.2V≥V_{IN}≥V_{CC}-0.2V, f=0	-	-	40	mA
Output Voltage Low	V_{OL}	I_{OL} = 8.0mA,V_{CC}=Min	-	-	0.4	V
Output Voltage High	V_{OH}	I_{OH} = -4.0mA,V_{CC}=Min	2.4	-	-	V

Notes: (1) $\overline{CS}$1~4 inputs operate simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.
(2) At f=f_{max} address and data inputs are cycling at max frequency.

Capacitance (V_{CC}=5V, T_A=25°C, F=1Mhz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance Address,$\overline{OE}$,$\overline{WE}$	C_{IN1}	V_{IN}=0V	-	-	32	pF
Output Capacitance 8-bit mode (worst case)	$C_{I/O}$	$V_{I/O}$=0V	-	-	38	pF

Note: These parameters are calculated, not measured.

AC Test Conditions

*Input pulse levels: 0.0V to 3.0V

*Input rise and fall times: 3 ns

*Input and Output timing reference levels: 1.5V

*V_{cc}=5V±10%

*PUMA module is tested in 32 bit mode.

Output Load

I/O Pin   166Ω

1.76V

30pF
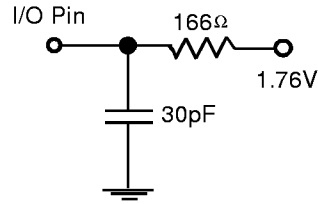
Operation Truth Table

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	$\overline{OE}$	$\overline{WE}$	SUPPLY CURRENT	MODE
L	H	H	H	X	L	I_{CC8}	Write $D_{0\sim7}$
H	L	H	H	X	L	I_{CC8}	Write $D_{8\sim15}$
H	H	L	H	X	L	I_{CC8}	Write $D_{16\sim23}$
H	H	H	L	X	L	I_{CC8}	Write $D_{24\sim31}$
L	L	H	H	X	L	I_{CC16}	Write $D_{0\sim15}$
H	H	L	L	X	L	I_{CC16}	Write $D_{16\sim31}$
L	L	L	L	X	L	I_{CC32}	Write $D_{0\sim31}$
L	H	H	H	L	H	I_{CC8}	Read $D_{0\sim7}$
H	L	H	H	L	H	I_{CC8}	Read $D_{8\sim15}$
H	H	L	H	L	H	I_{CC8}	Read $D_{16\sim23}$
H	H	H	L	L	H	I_{CC8}	Read $D_{24\sim31}$
L	L	H	H	L	H	I_{CC16}	Read $D_{0\sim15}$
H	H	L	L	L	H	I_{CC16}	Read $D_{16\sim31}$
L	L	L	L	L	H	I_{CC32}	Read $D_{0\sim31}$
X	X	X	X	H	H	$I_{CC32}/I_{CC16}/I_{CC8}$	$D_{0\sim31}$ High-Z
H	H	H	H	X	X	I_{SB},I_{SB1}	$D_{0\sim31}$ Standby

Notes : H = V_{IH} : L =V_{IL} : X = V_{IH} or V_{IL}

## AC OPERATING CONDITIONS

Read Cycle

Parameter	Symbol	-12 min	-12 max	-15 min	-15 max	-20 min	-20 max	-25 min	-25 max	Unit
Read Cycle Time	t_{RC}	12	-	15	-	20	-	25	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	-	25	ns
Chip Select Access Time	t_{ACS}	-	12	-	15	-	20	-	25	ns
Output Enable to Output Valid	t_{OE}	-	6	-	6	-	9	-	12	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	6	0	7	0	9	0	10	ns
Output Disable to Output in High Z	t_{OHZ}	0	6	0	7	0	9	0	10	ns

Write Cycle

| Parameter	Symbol	-12 min	-12 max	-15 min	-15 max	-20 min	-20 max	-25 min	-25 max	Unit
Write Cycle Time	t_{WC}	12	-	15	-	20	-	25	-	ns
Chip Selection to End of Write	t_{CW}	8	-	10	-	13	-	15	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	13	-	15	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width ($\overline{OE}$ high)	t_{WP1}	8	-	10	-	13	-	15	-	ns
Write Pulse Width ($\overline{OE}$ low)	t_{WP2}	12	-	12	-	14	-	15	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	6	0	7	0	9	0	10	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	9	-	10	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output active from end of write	t_{OW}	3	-	3	-	3	-	3	-	ns

Under Development

Read Cycle Timing Waveform [1,2]
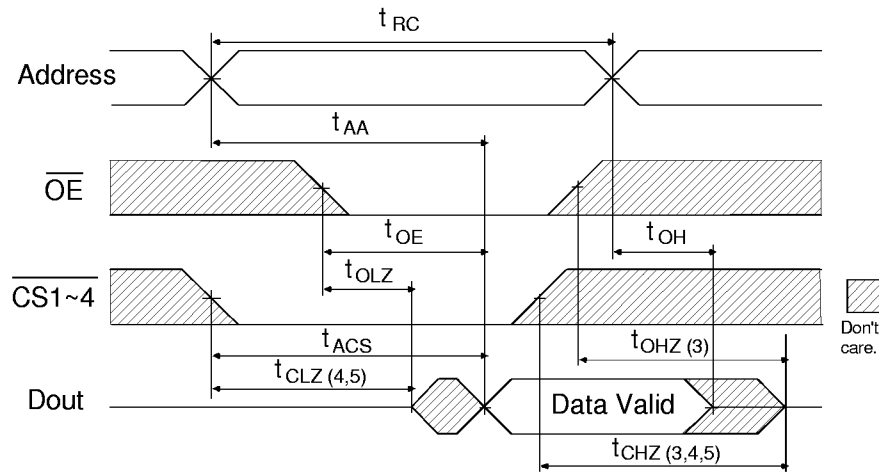
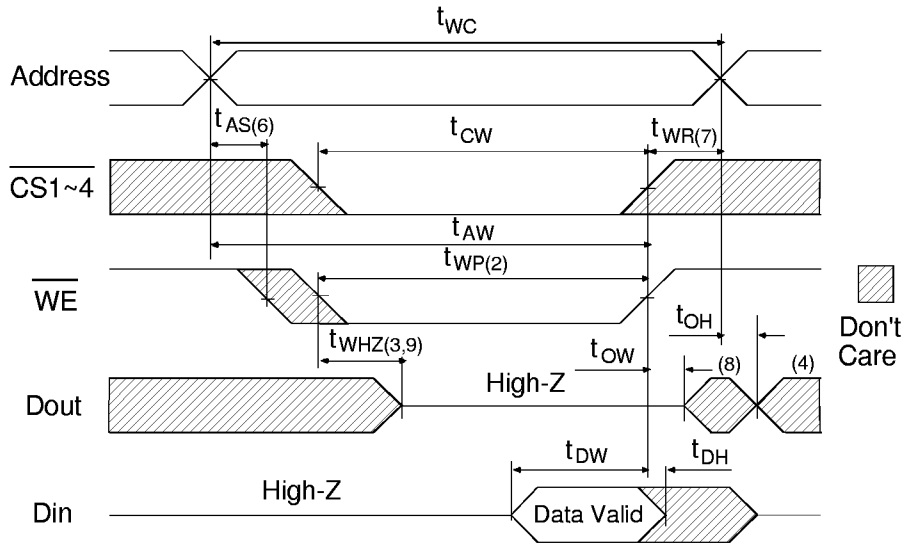### AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.

(2) All read cycle timing is referenced from the last valid address to the first transition address.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.

(4) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module and from module to module.

(5) These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform [1,4]
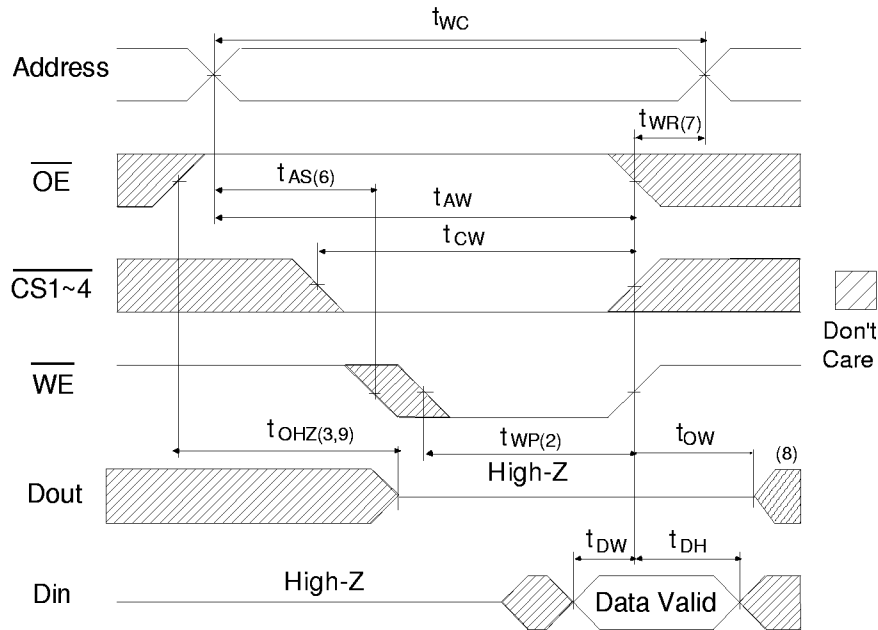
Write Cycle No.2 Timing Waveform [1,5]

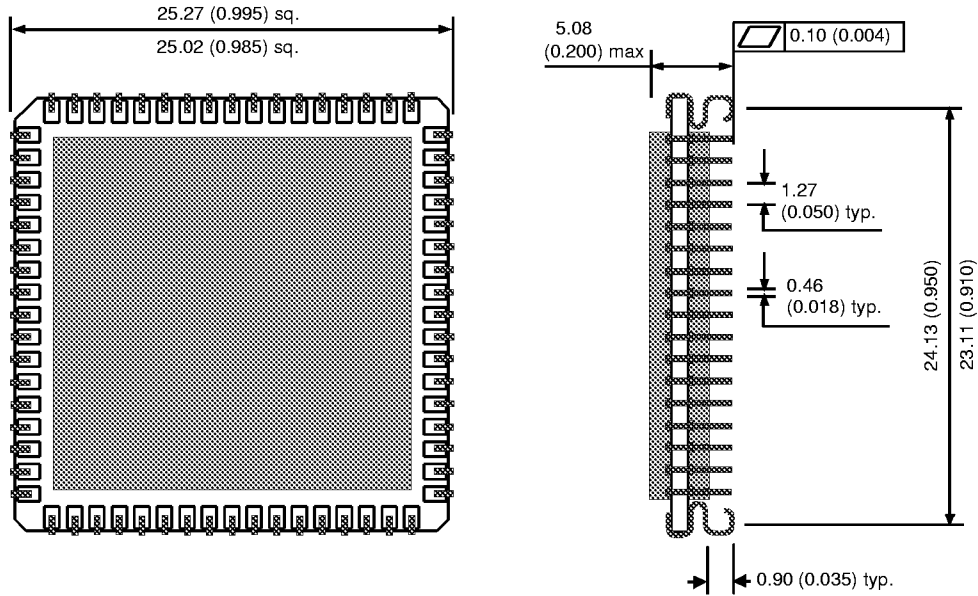## AC Write Characteristics Notes

(1) All write cycle timing is referenced from the last valid address to the first transition address.

(2) All writes occur during the overlap of $\overline{CS1\sim4}$ and $\overline{WE}$ low.

(3) If $\overline{OE}$, $\overline{CS1\sim4}$, and $\overline{WE}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.

(4) Dout is the Read data of the new address.

(5) $\overline{OE}$ is continuously low.

(6) Address is valid prior to or coincident with $\overline{CS1\sim4}$ and $\overline{WE}$ low, too avoid inadvertant writes.

(7) $\overline{CS1\sim4}$ or $\overline{WE}$ must be high during address transitions.

(8) When CS is low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.

(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.
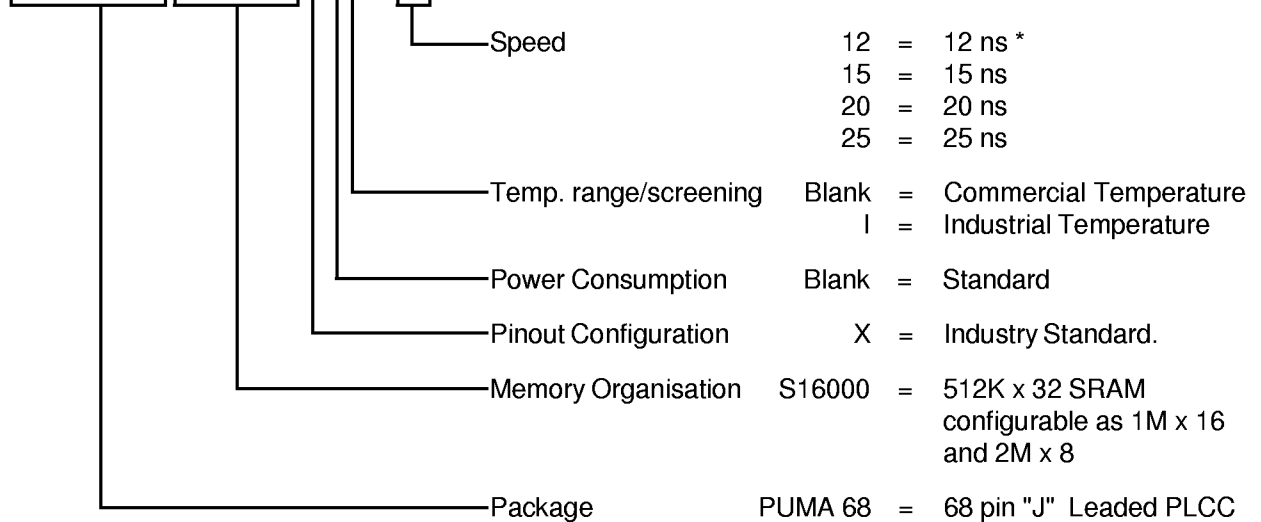
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Package Information   Dimensions in mm(inches)

Plastic 68 Pin JEDEC Surface mount PLCC

25.27 (0.995) sq.

25.02 (0.985) sq.

5.08
(0.200) max

0.10 (0.004)

1.27
(0.050) typ.

0.46
(0.018) typ.

24.13 (0.950)

23.11 (0.910)

0.90 (0.035) typ.

Ordering Information

PUMA 68S16000XLI - 15

Speed

12	=	12 ns *
15	=	15 ns
20	=	20 ns
25	=	25 ns

Temp. range/screening

Blank	=	Commercial Temperature
I	=	Industrial Temperature

Power Consumption   Blank   =   Standard

Pinout Configuration   X   =   Industry Standard.

Memory Organisation   S16000   =   512K x 32 SRAM
configurable as 1M x 16
and 2M x 8

Package   PUMA 68   =   68 pin "J" Leaded PLCC

* Under Development

Soldering Recommendations.

Bake.

    As specified on product packaging.

    If not specified HMP Ltd. recommend a minimum bake of 6 hours duration @ 125°C, if parts have been exposed to the atmosphere for 24 hours or more.

Soldering.

    Must not exceed,

        VPR 215 - 219°C, 60 secs.

IR / Convection   Ramp Rate 6°C/sec max.

                      Temp maintained at 125°C,120 secs max.

                      Temp exceeding 183°C, 120 - 180 secs.

                      Time at max. temp. 10 - 40 secs.

                      Max temp. 220 +5/-0°C

                      Ramp down -6°C/sec max.